

HIGH SPEED LOW POWER INPUT BUFFER

Abstract of the Disclosure

The input buffer circuit includes an input stage providing a switching point
5 voltage based on a predetermined switching point set between a first and second
reference voltages that maximizes the high and low noise margins of the input
buffer. The input buffer circuit further includes an output stage. The output stage is
coupled to the input stage. The output stage receives the switching point voltage
from the input stage and amplifies the switching point voltage to a full logic level
10 voltage.